4H-Silicon Carbide Schottky Barrier Diodes for Microwave Applications

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***Abstract*—In this paper, physical models for vertical 4H-silicon carbide (4H-SiC) Schottky diodes are used to develop a design method, where a maximum cutoff frequency for a given punch-through is achieved. The models presented are also used to extract microwave simulator computer-aided design (CAD) models for the devices. A device process was developed and Schottky diodes were fabricated in-house. Characterization of the devices was performed and compared to the theoretical models with good agreement. A demonstrator singly balanced diode mixer was simulated using the developed models. The mixer was fabricated using the in-house developed diodes, and measurements on the mixer show good agreement with the CAD simulations. A conversion loss of 5.2 dB was achieved at 850 MHz, and an excellent IIP_3 of 31 dBm at 850-MHz RF was measured, at 30-dBm P_{LO}. These results verify the enhanced properties of the SiC Schottky diode compared to other nonwide bandgap diodes.**

***Index Terms*—Device modeling, microwave mixers, Schottky barrier diode (SBD), silicon carbide (SiC).**

I. Introduction

In THE NEXT generation of mobile communication systems, multicarrier modulation schemes are used. The demands on the linearity of circuits, like the frequency mixer, are then increased. One-way of increasing the linearity is to use high-level local oscillator (LO) signals. It is therefore desired to combine high-frequency operation with high-power (or high-level) operation. In order to comply with such specifications, the use of devices fabricated in wide-bandgap materials such as silicon carbide (SiC) is a viable option. SiC devices take advantage of material properties such as a wide bandgap (3.25 eV) [1], a high critical field (2.5 MV/cm) [2], a high electron saturation velocity ($2.2 \cdot 10^7$ cm/s) [3], and a high thermal conductivity (4.8 W/cm/K) [4].

Most work on microwave wide-bandgap semiconductor devices today is focused on power transistors, for instance, [5]. However, microwave diodes are widely used for frequency translation in the microwave industry. One circuit that takes advantage of the unique material properties of SiC is the high-level diode mixer. A high-level mixer is an interesting component in communication systems, mainly since the third-order intermodulation is inversely proportional to the sixth power of the LO current [6], making circuits with very low intermodulation distortion (IMD) possible at the cost of high-input LO power. Handling high-power signals normally requires an increased number of switching elements in the mixer when using conventional GaAs or Si Schottky diodes, making the design and fabrication complex.

In the recent decade, 4H-SiC has developed to be a more mature and characterized material. Schottky contacts to SiC have been thoroughly investigated regarding their transport mechanisms and barrier height. At the same time, measurements of mobility, effective masses, and shallow donor levels have made it possible to calculate the conductivity theoretically for a given doping. Investigations of the breakdown related to avalanche multiplication gives the possibility of calculating the critical field or breakdown voltage for a given device. Using the published results and models (Section III), we investigate one way of optimizing the 4H-SiC Schottky barrier diodes (SBDs) for maximum cutoff frequency. That is, we build an equivalent circuit for the diode based on theoretical results and measurements of physical quantities. By comparing the theoretical and measured results (Section IV), we are able to verify the models. By doing this we are able to go from basic solid-state physics, via device design, to achieve models usable in circuit design. It is important to point out that a microwave SiC SBD differs considerably in the epitaxial-layer (device structure) design from a high-voltage SBD for which there has been numerous publications (see, for instance, [7]).

We demonstrate the potential of designing and modeling the SiC SBD in this way by designing and fabricating a simple singly balanced microwave mixer circuit using two of our diodes. This was the first SiC Schottky diode mixer published [8], although an SiC pn-diode mixer had been presented earlier [9].

II. Modeling the SBD

The structure of the vertical Schottky used in this work is shown schematically in Fig. 1. The equivalent circuit model for this structure consists of voltage-dependent elements (Fig. 2). In the small-signal case, the parallel coupled junction conductance $g_j(V)$ with the junction capacitance $c_j(V)$ in series with the series resistance $r_S(V)$ describes the device [see Fig. 2(b)]. In the large-signal case, the junction charge $Q_j(V)$ and the junction current $I_j(V)$ is used [see Fig. 2(a)], since the total current of the diode is simple to calculate as a function of junction voltage from these quantities.

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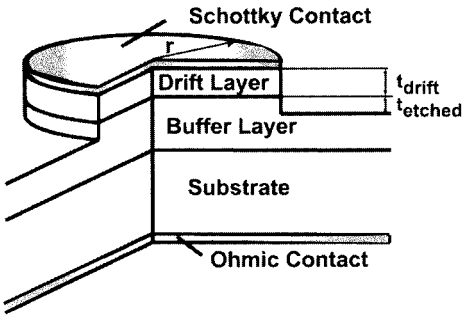


Fig. 1. Split view of the Schottky barrier structure.

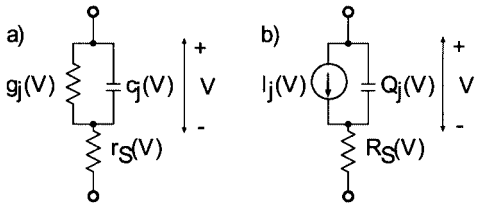


Fig. 2. (a) Small-signal circuit model and (b) large-signal circuit model for the SBD. V is the junction voltage.

A. Circuit Model Elements

In this section, the equations describing the elements in Fig. 2 are given. These equations may be used in microwave computer-aided design (CAD) systems for the design of microwave circuits.

1) Series Resistance R_S: The total series resistance of a diode structure as in Fig. 1 is due to the resistance in four regions; the quasi-neutral region ($R_{\rm QN}$), which is the nondepleted region of the drift layer, the buffer region ($R_{\rm buffer}$), the substrate region ($R_{\rm sub}$), and the ohmic contact (R_C). It is only the resistance of the quasi-neutral region that is voltage-dependent. By summing all four, we get the series resistance of the vertical SBD device [11]

$$R_S(V) = R_{\rm QN}(V) + R_{\rm buffer} + R_{\rm sub} + R_C. \tag{1}$$

The series resistance [see (1)] may be rewritten as

$$R_S(V) = \left(\frac{t_{\rm drift} - W(V)}{\sigma_{\rm drift}} + \frac{t_{\rm etched}}{\sigma_{\rm buffer}}\right)\frac{1}{\pi r^2} + \frac{1}{2\pi\sigma_{\rm sub} r} + R_C \tag{2}$$

where $t_{\rm drift}$ and $t_{\rm etched}$ are the thicknesses of the drift epi layer and the etched depth in the buffer epi layer respectively, $\sigma_{\rm drift}$, $\sigma_{\rm buffer}$ and $\sigma_{\rm sub}$ are the conductances for the drift epi, buffer epi ,and the substrate, respectively, and r is the radius of the Schottky contact.

We have neglected the difference between the conductance for the buffer and the substrate in the second-to-last term because the conductivities are almost equal. The depletion layer width $W(V)$ is given by

$$W = \sqrt{\frac{2\varepsilon_s}{qN_D}\left(V_{\rm bi} - V - \frac{k_B T}{q}\right)} \tag{3}$$

where q is the electron charge, $\varepsilon_s = 9.7\varepsilon_0$ is the dielectric permittivity of SiC, $V_{\rm bi}$ is the built-in potential, V is the applied voltage, k_B is Boltzmann's constant, T is the temperature in Kelvin, and N_D is the donor concentration.

For frequencies below 25 GHz and a diode radius of less than 50 μm, there is no need for skin depth correction to the series resistance equation, due to the greater skin depth of SiC compared to other materials with higher mobility.

The series resistance is calculated using a conductivity that depends on donor concentration, electric field (E), temperature, and the angle of the electron transport vectors to the c axis (θ). The conductivity is given by the product of electron charge (q), electron mobility (μ_n), and the number of free electrons (n) in the material

$$\sigma(N_D, E, T, \theta) = q \cdot \mu(N_D, E, T, \theta) \cdot n(N_D, T). \tag{4}$$

Using (5) and (6), we calculate the number of free electrons n which is used in (4).

The effective density of states (EDOS) in the conduction band is [12], [13]

$$N_c = 1.676 \cdot 10^{19}\left(\frac{T}{300}\right)^{3/2} \cdot \left(1 + \left(\frac{0.927}{0.764}\right)^{3/2}\exp\left(\frac{-0.12 \cdot q}{k_B T}\right)\right) \tag{5}$$

which, for $T = 300$ K, gives $N_c = 1.697 \cdot 10^{19}$ cm^{-3}.

We assume an n-type material, which implies that n is equal to the number of ionized donors N_D^+. The ionization grade for donors is found by solving the third degree equation (6) for n/N_D

$$\frac{n}{N_D} = \frac{N_{D,h}/N_D}{1 + g_c\frac{N_D}{N_c}\frac{n}{N_D}\exp\left(\frac{E_c - E_h}{k_B T}\right)} + \frac{N_{D,k}/N_D}{1 + g_c\frac{N_D}{N_c}\frac{n}{N_D}\exp\left(\frac{E_c - E_k}{k_B T}\right)}. \tag{6}$$

For the polytype 4H-SiC, there are one-half hexagonal donor sites and one-half cubic donor sites, which means $N_{D,h}/N_D = 1/2$ and $N_{D,k}/N_D = 1/2$, where N_D is the total donor concentration. The energy difference between the conduction band edge and the donor level for hexagonal and cubic sites are 52.1 and 91.8 meV, respectively [14], g_c is the donor level degeneracy factor which is equal to 2 for donors in SiC, and k_B is the Boltzmann constant. The percentage of ionized donors varies with temperature and doping (Fig. 3).

The low field mobility is strongly dependent on the concentration of donor atoms (Fig. 4). The Hall mobility of 4H-SiC follows the Arora model and has been experimentally determined [15] as

$$\mu_{n,\perp} = \frac{\mu_{\max}}{1 + \left(\frac{N_D + N_A}{N_{\rm ref}}\right)^{\gamma}}\left(\frac{T}{T_0}\right)^{\alpha} \tag{7}$$

where $\mu_{\max} = 947$ cm^2/Vs, $N_{\rm ref} = 1.94{\cdot}10^{17}$ cm^{-3}, $\gamma = 0.61$, $\alpha = -2.15$, and $T_0 = 300$ K.

The low field mobility is anisotropic for 4H-SiC. $\mu_{n,\perp}$ and $\mu_{n,||}$ are the mobility perpendicular and parallel to the c axis, respectively. The quota $\mu_{n,\perp}/\mu_{n,||}$ has been measured to be 0.83

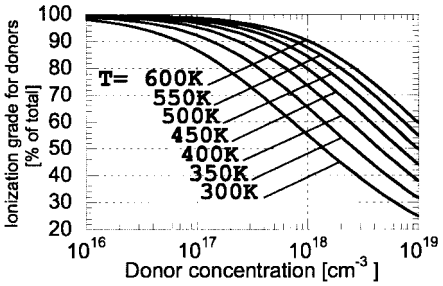


Fig. 3. Ionization grade versus donor concentration for different temperatures.

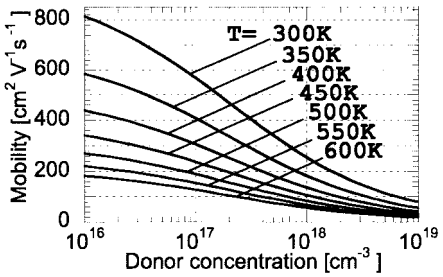


Fig. 4. Low field mobility versus doping for different temperatures. The mobility is given for transport perpendicular to the c axis.

[15]. The mobility for a given angle of the electron transport θ to the c axis of 4H-SiC is

$$\mu_n = \mu_{n,\perp}\sqrt{\left(\frac{\mu_{n,\parallel}}{\mu_{n,\perp}}\right)^2 \cos^2\theta + \sin^2\theta}. \tag{8}$$

If a point contact is assumed at a surface, the current that flows out from this point in a half sphere with basis at the surface has an average mobility value of $\mu_{n,\mathrm{avg}} = 1.09\mu_{n,\perp}$. This average value is used to compute the spreading resistance in the substrate.

2) Junction Charge/Junction Capacitance Model, $c_j(V)$ and $Q(V)$: The differential junction capacitance for a circular diode is [16]

$$c_j(V) = \frac{\partial Q}{\partial V} = \pi r^2 \sqrt{\frac{q\varepsilon_s N_D}{2(V_{\mathrm{bi}} - V - k_B T/q)}} \tag{9}$$

where Q is the charge in the semiconductor and $\varepsilon_s = 9.7\varepsilon_0$ is the dielectric permittivity of SiC. The charge $Q_j(V)$ associated with the junction capacitance is given in [11] by integrating (9) with respect to the voltage

$$Q_j(V) = -2c_{j0}(V_{\mathrm{bi}} - k_B T/q)\sqrt{1 - \frac{V}{V_{\mathrm{bi}} - k_B T/q}} + Q_0 \tag{10}$$

where c_{j0} is the zero-bias differential junction capacitance and Q_0 is an arbitrary integration constant.

The flat band barrier height ϕ^0_{bn} and the doping of the drift epilayer (N_D) determines the built-in voltage (V_{bi})

$$V_{\mathrm{bi}} = \phi^0_{\mathrm{bn}} - \frac{k_B T}{q}\ln\left(\frac{N_c}{N_D}\right). \tag{11}$$

These models are valid for $V < (V_{\mathrm{bi}} - k_B T/q)$. For $V > (V_{\mathrm{bi}} - k_B T/q)$, no simple model exists. To determine the capacitance for this case, the transport equations hasve to be solved together with the Poisson equation.

3) Current Density/Incremental Conductance Model, $I_j(V)$, $g_j(V)$: The current density using thermionic emission theory is [16]

$$J_j(V) = A^* T^2 \exp\left(\frac{-\phi_{\mathrm{bn}}}{k_B T}\right)\left(\exp\left(\frac{qV}{\eta k_B T}\right) - 1\right) \tag{12}$$

where $A*$ is the Richardson constant, ϕ_{bn} is the barrier height, and η is the ideality factor. If the current transport is thermionic, η is equal to unity, but the ideality factor is often greater than one, due to the tunneling current. A good SBD has an ideality factor of less than 1.2. Equation (12) is a good approximation for the current of a forward-biased 4H-SiC SBD [22]. The incremental conductance $g_j(V)$ for a circular diode is [11]

$$g_j(V) = \frac{\partial I_j(V)}{\partial V} = \pi r^2 \frac{\partial J_j(V)}{\partial V}. \tag{13}$$

In the case of a forward-biased diode where the transport is dominated by thermionic emission [17], $g_j(V)$ is

$$g_j = \frac{\pi r^2 A^* q T}{\eta k_B}\exp\left(\frac{-\phi_{\mathrm{bn}}}{k_B T}\right)\exp\left(\frac{qV}{\eta k_B T}\right). \tag{14}$$

When the diode is reverse biased, the tunneling current contribution cannot be neglected. $g_j(V)$ and $J_j(V)$ are then evaluated using a numerical evaluation of (15). The total current including the tunneling current is calculated using the WKB approximation to a parabolic barrier given by the depletion approximation [18]. Furthermore, image force lowering of the barrier is introduced.

We assume that the current in the depletion region is relatively low. The few carriers present will therefore not perturb the potential. The use of the potential of the depletion approximation is then justified. The reverse current density is

$$J = \frac{A^* T}{k_B} \times \int_0^\infty T(E) \times \ln\left(\frac{1 + \exp[(-qV_n - E)/k_B T]}{1 + \exp[(-qV_n - qV - E)/k_B T]}\right) dE \tag{15}$$

where

$$qV_n = E_c - E_F. \tag{16}$$

Using the effective masses from [12], the Richardson constant (A^*) is calculated to be 151 A $\cdot$ cm$^{-2}\cdot$K^{-2}.

The tunneling probability has a closed-form expression [18]

$$T(E) = \exp\left[\frac{2}{\hbar q}\sqrt{\frac{m_c^* \varepsilon_s}{N_D}} \times \left(E\ln\frac{\sqrt{E_b^*} + \sqrt{E_b^* - E}}{\sqrt{E}} - \sqrt{E_b^*}\sqrt{E_b^* - E}\right)\right] \tag{17}$$

where

$$E_b* = q(V_{\mathrm{bi}} - V). \tag{18}$$

Image force lowering (IFL) is included in this approximation by modifying the barrier height at the interface [19]

$$\phi_{\rm bn}^{0} = \phi_{\rm bn} + \Delta\phi_{\rm bn}. \tag{19}$$

where $\Delta\phi_{\rm bn}$ is the image force lowering.

The IFL adjustment of the barrier height is

$$\Delta\phi_{\rm bn} = \left(\frac{q^7 N_D}{8\pi^2(\varepsilon_S')\varepsilon_S}\left(V_{\rm bi} - V - \frac{k_B T}{q}\right)\right)^{1/4} \tag{20}$$

where $\varepsilon_S' = 6.7\varepsilon_0$ is the high-frequency dielectric permittivity of the silicon carbide.

B. Breakdown Voltage

It is often desired to drive the component material to its limits, e.g., achieve voltages as high as possible in the reverse direction before breakdown. The critical field (E_{cr}) for materials with doping concentrations of $10^{15} < N_D < 10^{18}$ cm^{-3} is calculated using [2]

$$E_{\rm cr} = \frac{E_{\rm cr,\,ref}}{1 - \frac{1}{4}\log_{10}(N_D/N_{\rm ref})} \tag{21}$$

where $E_{\rm cr,\,ref}$ is $2.49 \cdot 10^6$ V/cm, and $N_{\rm ref}$ is 10^{16} cm^{-3}. The breakdown voltage is then given by [16]

$$V_B = \frac{qN_D W^2}{2\varepsilon_s} - V_{\rm bi} = \frac{\varepsilon_s E_{\rm cr}^2}{2qN_D} - V_{\rm bi}. \tag{22}$$

III. Microwave Optimization

The cutoff frequency is defined as

$$f_c = \frac{1}{2\pi C_{j0} R_S} \tag{23}$$

where C_{j0} is the junction capacitance at zero bias and R_S is the series resistance of the device. It is widely regarded as a figure of merit, and it is important for varistor applications.

Using the equations of breakdown voltage, punch-through voltage, series resistance, and junction capacitance, we can optimize the structure for maximum cutoff frequency for a given punch-through voltage.

The drift-layer thickness is designed to reach punch-through (depletion of the entire drift-layer thickness) at the chosen (selected) reverse operating voltage. The upper limit for the doping concentration of the active (top) epilayer for this voltage is determined, by calculating the breakdown voltage versus doping (Fig. 5) from (21) and (22). If the doping is higher, avalanche breakdown will occur before the punch-through voltage of the drift epilayer is reached. If the doping is lower, the punch-through voltage device will reached first. We choose a doping concentration below the upper limit. The depletion layer width from (3) then gives the desired thickness for the top epilayer using the design voltage and doping concentration (level) from above (Fig. 6).

The depletion width is used to calculate the junction capacitance c_j [see (9)] and the series resistance R_S [see (2)]. The cutoff frequency is then calculated using (23). The exact choice of the doping concentration for the design will later be determined by the doping that gives the highest cutoff frequency. Different choices of doping/thickness will give different series resistance and capacitance and, consequently, different cutoff frequencies.

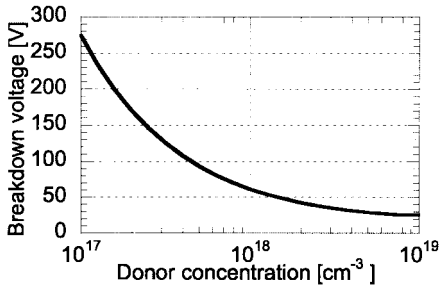


Fig. 5. Breakdown voltage versus doping.

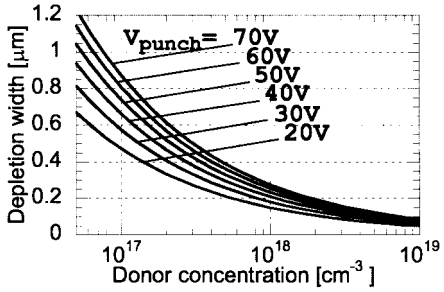


Fig. 6. Depletion width versus doping. The different curves are for different punch-through voltages.

Two diagrams (Figs. 7 and 8) are given for the cutoff frequency optimization, with radius and doping used as the variables, respectively. A buffer thickness and doping of 0.5 μm and $8 \cdot 10^{18}$ cm^{-3}, respectively, and a substrate doping of $1 \cdot 10^{19}$ cm^{-3} are assumed. In the figures, a maximum reverse voltage of 50 V before punch-through is also assumed. The substrate and buffer are not considered in the breakdown calculations, since the depletion region should not extend into these regions, and hence most of the voltage drop is over the top drift layer.

The highest cutoff frequency is achieved for low doping and a small radius (Figs. 7 and 8). However, depending on the radius of the diode, the doping that gives the maximum in the cutoff frequency varies between $2 \cdot 10^{16}$ and $2 \cdot 10^{17}$ cm^{-3} for radii of 50 to 5 μm (Fig. 8). For diodes that will be contacted with bond wires, a radius of at least 10 μm is required.

For a 10-μm radius device, the maximum cutoff frequency is 83 GHz is given for a doping of $5 \cdot 10^{16}$ cm^{-3}. Schottky diodes in circuits are usually used well below their cutoff frequency. If the cut off is 10 times higher than the operating frequency of the circuit, the model is very good. Basically, the further the device is operated below the cutoff frequency, the better the model (Fig. 2) works. Using (3) (Fig. 6), the thickness of the layer should be 1.05 μm. The reverse current is calculated, using (15). Assuming that a titanium (Ti) Schottky diode is used with a barrier height of 0.88 eV and the previously determined doping, the reverse current is calculated to be 2 μA at a reverse voltage of 50 V.

In a mixer or multiplier circuit, the series resistance is an important parameter since it determines the conversion loss and

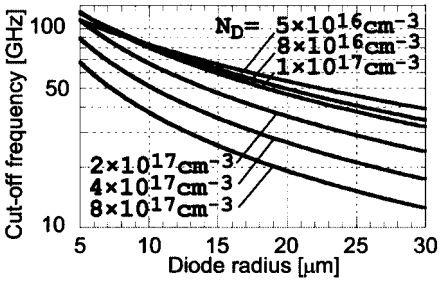


Fig. 7. Cutoff frequency versus radius (step doping).

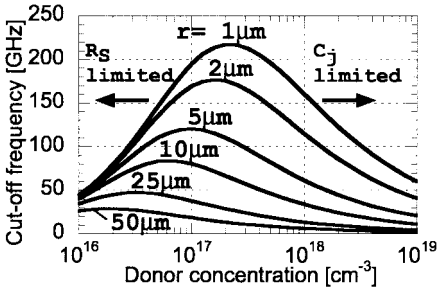


Fig. 8. Cutoff frequency versus doping (step radii).

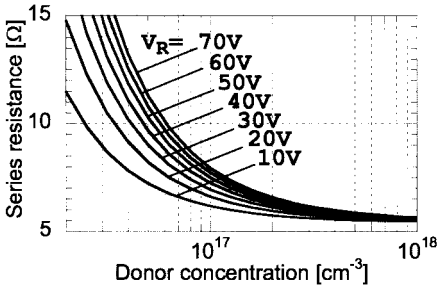


Fig. 9. Series resistance (R_S) as a function of N_D, $r = 10\mu$m, $t_{\rm drift}$ = depletion width at punch-through for a reverse junction voltage of V_R. R_S is given at $V = 0$ V.

limits the current. It may thus be better to lower the series resistance, even if this also means reducing the cutoff frequency. Fig. 9 shows the series resistance for a diode with a radius of 10 μm with different design alternatives in doping and punch-through voltage.

In conclusion, this optimization for a 50-V punch-through, 10-μm radius Schottky diodes give a device with a maximum leakage current of 2 μA and a cutoff frequency of 83 GHz. The zero-voltage junction capacitance c_{j0} is 0.19 pF, $c_{j,\min}$ is 26 fF, and the series resistance $R_S(0\ \text{V}) = 10.2\ \Omega$.

IV. Experimental Investigation of the 4H-SiC SBD

The material available at the time of diode fabrication was not the material optimized for in the previously given example. However, diodes fabricated on a nonoptimal material that is similar in structure can verify the models and principles of the design method and (as will be presented in the following sections) used to build a demonstrator mixer.

A. Device Structure and Processing

The SBD is described in Fig. 1. All epi-layers and the substrate are n-type. The doping concentration for the drift layer, buffer layer, and substrate is $2.8 \cdot 10^{17}$ cm^{-3}, $8 \cdot 10^{18}$ cm^{-3}, and $1.1 \cdot 10^{19}$ cm^{-3}, respectively. The drift layer, buffer layer, and substrate are 0.38, 0.5, and 340 μm thick, respectively.

The epi-layers and the Schottky contact was grown and deposited on the Si-face of the wafer. Mesas are etched by ion beam etching (IBE) with Ar using Ti as an etch mask, which was removed after the etching. The sample was cleaned using $H_2SO_4 : H_2O_2$ (3 : 1) for five minutes and also by the RCA Standard Cleans. Schottky barriers are formed by lift-off of evaporated of Ti–Au. Prior to Schottky contact evaporation, the sample was dipped in diluted (4%) HF for 10 s. A backside contact was formed by Ni-evaporation and annealing at 950 °C for 5 min in $Ar : H_2$ (10 : 1) atmosphere. Finally, the backside was gold-plated.

B. Results

Measurements of the resistance for several different radii give the following curve fit equation:

$$R_S = 105.5r^{-2} + 52.2r^{-1} + 0.27 \quad [\Omega] \tag{24}$$

where r is given in micrometers.

Using a backside area of 8 × 8 mm, we can calculate the specific contact resistance ρ_C to be $4 \cdot 10^{-1}$ Ωcm^{-2}. This value is several magnitudes worse than what should be expected from an optimized ohmic contact process ($<10^{-4}$ Ωcm^{-2}). However, the contact resistance is small for most devices compared to the spreading resistance for the substrate. In the theoretical predictions, an optimized process with negligible R_C was assumed. Theoretically the series resistance is given by (2), and inserting measured temperature, thicknesses, and dopings gives

$$\begin{aligned} R_S &= 95.2r^{-2} + 53.2r^{-1} \quad [\Omega] \\ T &= 300\ \text{K} \\ t_{\rm etched} &= 0.17\ \mu\text{m}. \end{aligned} \tag{25}$$

The $1/r$ term is the contribution from the substrate, and $1/r^2$ is contribution from the cylindrical portion of the device (Fig. 1). Considering the used processing methods, the $1/r^2$ term is the most uncertain and it is very possible that etch damage may have been induced that would render an effective $t_{\rm etched}$ close to 0.31 μm, which then would give

$$\begin{aligned} R_S &= 105.5r^{-2} + 53.2r^{-1} \quad [\Omega] \\ T &= 300\ \text{K} \\ t_{\rm etched} &= 0.31\ \mu\text{m} \end{aligned} \tag{26}$$

which is very close to the measured results [see (24)].

Measurements on 11 diodes with a radius of 50 μm showed (Fig. 10) a difference in capacitance of less than 1% for different diodes over the voltage swing of 0 to −40 V. The measured $V_{\rm bi}$ was 0.97 V and N_D was measured to be $2.8 \cdot 10^{17}$ cm^{-3}. This gives, by (11), a $\phi^0_{Bn} = 0.97 + 0.11 = 1.08$ eV. The capacitance scaled linearly to the diode area as predicted by theory (9), thus yielding

$$C_{j0} = 4.68r^2 \quad [\text{fF}] \tag{27}$$

for the measured capacitance.

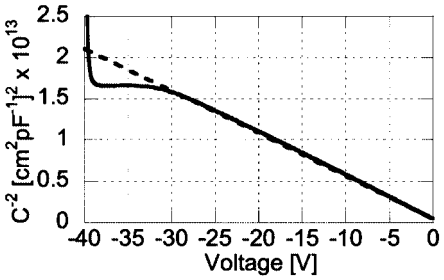


Fig. 10. Capacitance–voltage characteristics for the reverse-biased diode. The solid C–V curve shown represents the average of measurements on 11 diodes with an anode radii of 50 μm. The C_{j0} for these diodes were approximately 11.7 pF. The dashed line is modeled data for a constant doping of $2.82 \cdot 10^{17}$ cm^{-3}, and $V_{bi} = 0.97$ V.

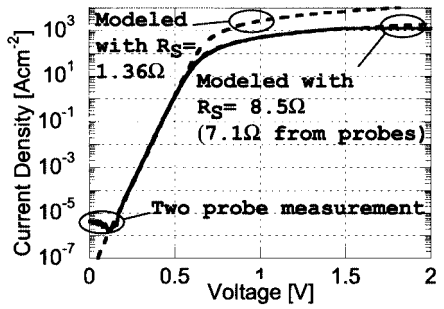


Fig. 11. Current–voltage characteristics for the forward biased diode. The line represents the average current–voltage curve for four diodes, with an anode radii of 50 μm. The dashed lines show modeled behavior for the device. The higher R_S value of 8.5 Ω is due to an added probe resistance of 7.1 Ω.

I–V measurements for voltages from 0.2 to 0.6 V gave a barrier height of $\phi_{Bn} = 0.88$ eV. It has been noted previously by others that there is a large difference of barrier heights extracted from I–V and C–V measurements [17], [20].

When the I–V value (ϕ_{Bn}^{I-V}) is used, and additional lowering by IFL ($\Delta\phi_{Bn}$) is added to the model (19), a good agreement between measured and theoretical prediction [see (12) and (15)] is achieved for both forward (Fig. 11) and reverse current (Fig. 12). In addition, a four-probe measurement on the diodes was made to accurately determine the series resistance, and it yielded the lower value of 1.36 Ω in Fig. 11. The higher value of 8.5 Ω included the probe resistance, which was 7.1 Ω. That measurement was also used to extract the curve-fit equation (24). The considerably lower barrier height for the I–V measurements compared to the C-V measurements can be explained by more advanced models taking a statistical distribution of the barrier height into account [21]. However, that approach, although it is more true to the real physics of the device, will give another fitting parameter to be determined, which is dependent on experimental values. The model we used can predict the reverse current with fair accuracy and the forward current with excellent agreement. The reverse current is overestimated by the model, especially for low voltages. The model only predicts the behavior in the drift layer and not the buffer layer, which is why we see the tails in Figs. 10 and 12 for the measured values.

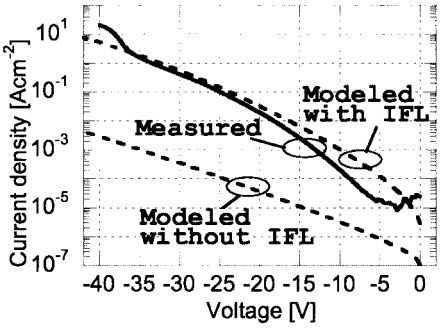


Fig. 12. Current–voltage characteristics for the reverse-biased diode. The line represents the average current–voltage curve for eight diodes with an anode radii of 50 μm.The dashed lines show the modeled characteristics.

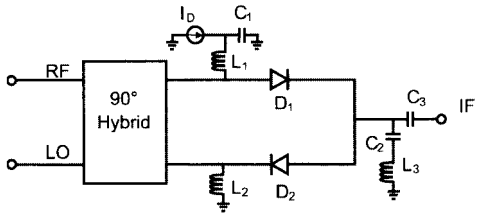


Fig. 13. Mixer topology.

TABLE I
CAD-MODEL PARAMETERS FOR A 40 × 40 μm SBD

Element	Value
I_{j0}	0.5 pA
R_S	2.5 Ω
C_{jo}	2.4 pF
V_{bi}	0.97 V
η	1.08

V. MIXER DESIGN

A. Design and Experimental Setup

The mixer was designed at a low frequency (850 MHz) with relatively large square diodes (40 × 40 μm) to facilitate a quick fabrication of the circuit. The singly balanced mixer was chosen since it is a simple circuit with fewer possible error sources compared to a more complex design with smaller diodes.

The topology of the singly balanced diode mixer circuit [11] is shown in Fig. 13. The mixer was designed for minimum conversion loss (CL) using a commercial microwave CAD program (Microwave Design System (MDS), Agilent). The diodes were modeled using the parameters in Table I. These parameters were extracted from (24) and (27) (Figs. 10 and 11).

The mixer consists of two diodes (D_1 and D_2) combined with a 90°-hybrid. The LO and RF are applied to two mutually isolated ports. The diodes are connected to the other ports with opposite polarity. The bias current is fed through two inductors (L_1 and L_2) working as RF chokes. The capacitor C_1 is used for dc blocking and decoupling. The capacitors (C_2 and C_3) and inductor (L_3) at the IF port is a low-pass filter and dc block. The mixer was fabricated on a duroid-substrate mounted on a copperplate. Chip capacitors and inductors were soldered to the

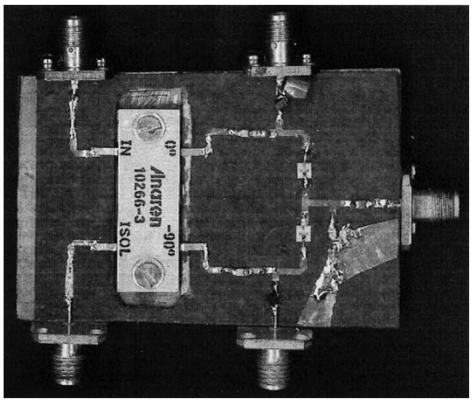


Fig. 14. Photograph of the mixer.

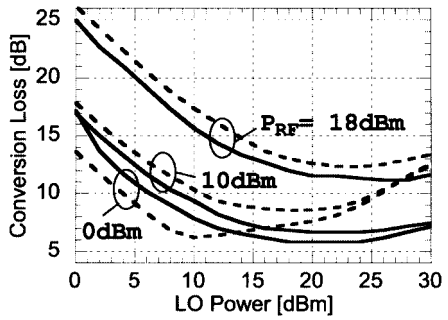


Fig. 15. Conversion loss versus LO power. Curves are given for three different RF powers. Solid lines are measurements, and dashed lines are simulations.

substrate. The diodes were diced and soldered and bonded on an alumina-carrier. The carriers were then glued to the substrate and wire bonded to the circuit. SMA contacts were used for the RF, LO, IF, and dc connections.

The diodes were biased with a constant current and the measurements were performed at an RF of 850 and 1280 MHz, since these frequencies give a minimum CL and highest LO-to IF-port isolation, respectively.

B. Results

In this section, the performance of the mixer (Fig. 14) is presented and compared to harmonic balance simulations. In the simulations, the predefined MDS diode model was used with the model parameters given in Table I. Because of the high power levels both for the LO and the RF signals, oversampling and additional harmonics were used to make the simulation converge and give reliable results. This is especially important for the intermodulation simulations.

In Fig. 15, the CL versus LO power ($P_{\rm LO}$) measurements at different RF powers ($P_{\rm RF}$) are given. The diode mixer operated at a bias current 5 mA, an LO frequency of 800 MHz, and an RF frequency of 850 MHz.

The CL dependence on diode bias current (I_D) was measured (Fig. 16). The optimum I_D for minimum CL is 4–15 mA depending on the input power. Higher I_D is required at higher power levels to achieve minimum conversion loss. CL versus RF was measured (Fig. 17) and simulated for a $P_{\rm LO}$ of 20 and 25 dBm. I_D was 5 mA in all resulting points, i.e., I_D was not optimized for minimum CL. The lowest conversion loss is

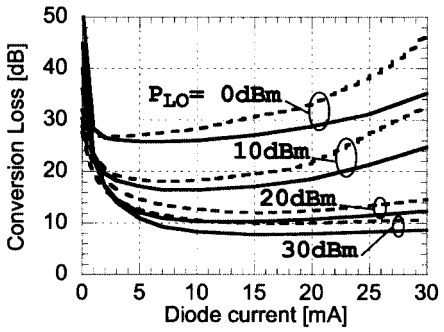
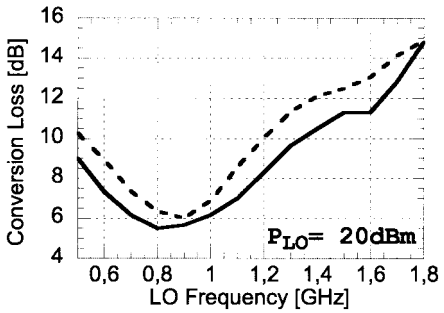
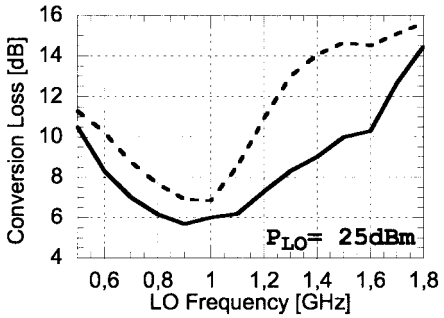


Fig. 16. Conversion loss versus bias current for $P_{\rm RF} = 18$ dBm. The $f_{\rm LO}$ was 1330 MHz. Curves are given for four different LO powers. Solid lines are measurements, and dashed lines are simulations.



(a)



(b)

Fig. 17. CL versus RF. $P_{\rm LO}$ is: (a) 20 dBm, and (b) 25 dBm, $P_{\rm RF}$ is 0 dBm, $f_{\rm IF}$ is 50 MHz, and I_D is 5 mA. Solid lines are measurements, and dashed lines are simulations.

achieved at 850–950 MHz (Fig. 17). The CL 3-dB bandwidth is ~800 MHz at 950 MHz and a $P_{\rm LO}$ of 25 dBm. The frequency for minimum conversion is increasing with increasing $P_{\rm LO}$. This frequency shift is partly explained by the nonoptimum I_D. The lowest CL was measured to be 5.2 dB at an I_D of 15 mA, an RF of 800 MHz, and a $P_{\rm LO}$ of 25 dBm. For comparison with other SiC-diode mixers, our mixer has a CL of 5.5 dB at 850 MHz, compared to 12 dB at 500 MHz in [10].

A two-tone measurement was used to determine the third-order intercept point ($\rm IIP_3$). The equal-power RF input signals are separated by 10 MHz. Special attention was paid to keep the noise floor of the LO and RF signals at a low level, making it possible to measure IMD for a wide range of $P_{\rm LO}$ and $P_{\rm RF}$. The intermodulation of the mixer was measured for different I_D, and $\rm IIP_3$ is plotted for these measurements in Fig. 18. The highest $\rm IIP_3$ for this mixer is 31 dBm at 850 MHz and a current of 15 mA (Fig. 19).

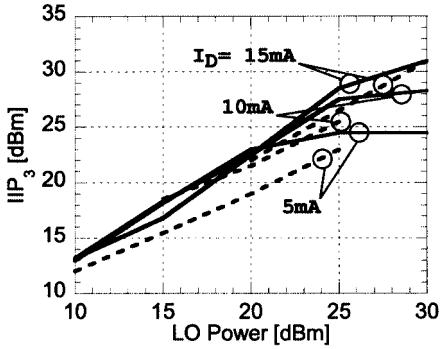


Fig. 18. Third-order intermodulation input intercept point (IIP_3) versus input P_{LO}. Curves are given for three different bias currents. Solid lines are measurements and dashed lines are simulations.

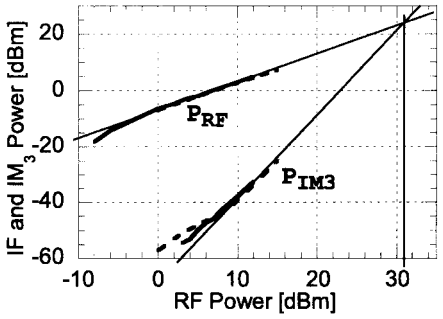


Fig. 19. IF Power and IM_3 Power versus RF Power. LO power is 30 dBm, I_D is 15 mA, f_{LO} is 800 MHz, and f_{RF} is 800 MHz. The supporting lines show the 31 dBm IIP_3. Solid lines are measurements and dashed lines are simulations.

VI. Discussion and Conclusion

Models for the 4H-SiC SBD have been given. References and given parameters can also be used to implement models for use in a physics-based device simulator. The measured current shows a significant deviation from the most simplistic theory, where there is a simple relationship between the C–V (ϕ_{Bn}^{C-V}) and I–V (ϕ_{Bn}^{I-V}) barrier heights. Regions within the Schottky diodes with different barrier height can explain this deviation, and it must be accounted for by using measured Schottky barrier heights for C–V and I–V. If this is done, the models give very good fits to measured results. It should also be noted that the models for the reverse current also agrees well with the theoretical predictions. Small- and large-signal models based on the physical models have been given and are used in a commercial CAD program. This shows the maturity of physical models and model parameters and how far they can be taken. It is an important step forward that we now can use physical models to predict the device behavior with such accuracy that the models can be used in a CAD circuit simulator to produce simulation results very close to measurements.

Using the equations and relationships given in this paper, it is also straightforward to optimize the microwave Schottky diode for maximum cutoff frequency with a relatively small computational effort. In this paper, we have shown, an optimization of cutoff frequency for cases, where the diode is used as a varistor, such as in, for instance, in a mixer or limiter. However, when designing frequency multipliers, the diode is used as a varactor and the dynamic cutoff frequency is more appropriate [11] as follows:

$$f_{cd} = \frac{1}{2\pi R_S}\left(\frac{1}{C_{j,\min}} - \frac{1}{C_{j,\max}}\right). \tag{28}$$

The feasible large reverse voltage in combination with a large voltage swing gives a small $C_{j,\min}$, compared to other semiconductor materials with the same drift layer doping. Compared to GaAs Schottky diodes, the cutoff frequency is still low, but a 4H-SiC SBD can handle more power due to the higher critical field and thermal conductivity. Thus, 4H-SiC SBDs may be well suited for frequency multipliers and mixers where high output power is desired. It should be noted that the above figures of merit assume a constant series resistance. As we know from the theory above, it is both voltage-dependent and frequency-dependent. Often the maximum series resistance is used (at $V_F = V_{\mathrm{bi}}$) or the value it has at zero volts bias. This could easily be investigated using a similar approach as the one we have taken in this paper.

A singly balanced SiC Schottky diode mixer was designed and characterized with results that show the advantages of using an SiC Schottky diode. A conversion loss of 5.2 dB and an IIP_3 of 31 were measured at 850 MHz. To our knowledge, these are the best-reported results for a SiC mixer. These results show the good progress of SiC theory and technology.

Acknowledgment

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